Total No. of printed pages = 4

ET 131304

Roll No. of candidate | | | | | | | | | | |

2017

B.Tech. 3rd Semester End-Term Examination

Computer Science Engineering

DIGITAL SYSTEMS

Full Marks – 100 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Question No. 1 and any *six* from the rest.

1. Fill in the blanks :

   (a) 9's complement of no 5968 is ————————.

   (b) In a K map, iff all the cell contains 1, the output becomes ————————.

   (c) The octal equivalent of $(10111011)_2$ is ————————.

   (d) Binary equivalent of (1101101) grey is ————————.

   (e) In a X-OR gate, O/P is high only when both the inputs are ————————.

   (f) Fastest among logic families is ————————.

[Turn over

(g) Race around condition occurs when J = ———— and K = ————.

(h) A simple flip-flop is a ———— bit memory.

(i) In positive logic 5 V is considered as ————.

(j) To design a MOD 5 synchronous counter, no of flip flop requires is ————.

2. (a) Convert the decimal no $(98)_{10}$ into (5)

(i) Binary code

(ii) Grey code

(iii) BCD code

(iv) Excess 3 code

(v) Octal code

(b) Find the base x

$(107)_{10} = (153)_x$ (3)

(c) Perform the binary addition (2)

$$\begin{array}{r} 110110 \\ +\ 110001 \\ +\quad 111 \\ \hline \end{array}$$

(d) Using 2's complement $(23)_{10}$ from $(46)_{10}$. (5)

3. (a) Realize NAND gate using only NOR gate. (5)

(b) Prove using Boolean algebra

$AB + \overline{A}C = (A + C)(\overline{A} + B)$. (5)

(c) Implement the following expression using only NAND gate $Y = A\overline{B}C + B\overline{C} + \overline{D}$. (5)

4. (a) Simply using K map

$Y = \Sigma m(0,1,2,3,5,7,10,13,15)$. (5)

(b) Perform the following BCD addition. (5)

(i) $(679.6)_{10} + (536.8)_{10}$

(ii) $(342.8)_{10} + (108.9)_{10}$.

(c) Expand $Y = ABC + \overline{B}CD + BD$ to minterm and maxterm. (5)

5. (a) Draw the logic diagram of full adder using two half adder. Justify with logic expression starting from the truth table. (5)

(b) Design a two bit comparator. (5)

(c) Design a 8:1 MUX using 4:1 MUX and 2:1 MUX. (5)

6. (a) Explain Race around condition. How it can be avoided?

(b) Convert SR FF into JK FF. (5)

(c) What is parity generator? Design an even parity generator. (5)

7. (a) What is counter? Explain different types of triggering. (2)

(b) Differentiate between asynchronous and synchronous counter with suitable diagram. (3)

(c) Explain the operation of ring counter with neat diagram. (5)

(d) What is shift register? What are the modes of operation of a shift register? Explain. (5)

8. (a) Draw the circuit diagram of TTL NAND gate and explain its operation. (8)

(b) Minimise the following expression using Quine-Mc-Clusky method.

$F = \Sigma m(0, 2, 3, 5, 7, 8, 12, 13)$. (7)

9. (a) Design a MOD 5 synchronous counter using JK flip flop and implement it. (10)

(b) Write short notes on : (5)

(i) FPGA

(ii) ROM.