Total No. of printed pages = 4

EC 131703

Roll No. of candidate | | | | | | | | | | |

2017

B.Tech. 7th Semester End-Term Examination

Electronics and Communication

VLSI DESIGN

Full Marks – 100 Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No. 1 and any *Six* from the rest.

1. Fill in the blanks : $(10 \times 1 = 10)$

   (a) In an n MOSFET the substrate is of ———— type.

   (b) At ———— voltage, the MOSFET enters into the saturation region of operation.

   (c) ———— technique is used for controlled doping in narrow region.

   (d) γ is ———— in p MOS.

   (e) ———— is used for wet oxidation.

   (f) Deposition of SiO_2 film is mainly done by ———— process.

   (g) The equivalent resistance of a switched capacitor is ———— proportional to the clock frequency.

[Turn over

(h) FPGA-based design has turn-around time ———— than ASIC based design.

(i) PLA has ———— AND plane followed by a programmable OR plane.

(j) SPLD contains ———— elements like F/F.

2. (a) Explain the working of an n type MOSFET in enhancement mode with suitable diagram. (6)

(b) Derive expression for current in MOSFET operating in linear region. (4)

(c) What is threshold voltage? Calculate the body co-efficient (γ) of an n MOSFET that has a gate oxide thickness tox = 120 A_O. The p bulk region is doped with Na = 8×1014/cm3. Given W/L = 10 and Vth = 0.7 V? (5)

3. (a) What is flat-band voltage? Explain the hole accumulation region in the energy band diagram of a MOSFET. (5)

(b) What is figure of merit? Calculate the figure of merit of an nMOS transistor with following parameters : $W = 2\mu m$, $L = 0.2\ \mu m$, $t_{OX} = 200$, $\varepsilon_{SiO_2} = 4.0$, $V_{th} = 0.7\,V$, $V_{gs} = 1.0\,V$, $\mu_n = 660\ cm^2/Vs$. (5)

(c) What are the different MOSFET capacitances? Explain with proper diagram. (5)

4. (a) Show the fabrication process of an n channel MOSFET with neat diagram. (7)

(b) Which metals are commonly used for metallization in IC fabrication process?

Why do we prefer to fabricate the gate (G) at first and then we fabricate the Source(S) and the drain (D) regions. (3)

(c) What is LOCOS? Explain with proper diagram? (5)

5. (a) Draw the SAH model and write the equation for the drain current. (3)

(b) What is Channel length modulation? (7)

(c) What is VHDL? Write a behavioural description of an SR flip flop. (5)

6. (a) Prove that the pull up to pull down ratio of an nMOS inverter driven by another inverter through a series of pass transistors is 8:1. (5)

(b) Explain how the combination of switches and capacitor can emulate a resistor. (5)

(c) What are the five distinct regions of operation of a CMOS inverter? (5)

7. (a) Draw the stick diagram of a XOR gate. (5)

(b) Write the scaling factors for the following : (5 × 2 = 10)

(i) Gate capacitance

(ii) Carrier density in the channel

(iii) Gate Delay

(iv) Current Density

(v) Power dissipation per gate.

8. (a) Calculate the dynamic power dissipation of a CMOS inverter operating at 200 MHz. The power supply voltage is 2.0 V and the load capacitances is 10 fF. If the delay through the inverter is 10 ps then calculate the PDP. (5)

(b) Design an nFET based 2 : 1 multiplexer. Discuss the limitation in it. Also draw its stick diagram. (7)

(c) Realise an XOR operation using CPTL. (3)

9. (a) How does a MOSFET behaves as a current source or current sink? (4)

(b) Explain with appropriate diagram, the operation of a FLASH ADC. (6)

(c) What is a transmission gate? Implement the given function using transmission gate. (5)

$F = ABC + A'C + BC'$

10. (a) What is pseudo n-MOS? Explain the PE dynamic logic with neat diagram. (5)

(b) Write short notes on any two of the following : $(2 \times 5 = 10)$

(i) CPLP

(ii) Back gate effect

(iii) CMOS Latch up

(iv) Czochralski method of water fabrication.