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SUBJECT CODE = INT052104

Roll No. of candidate

2017

End Semester B.Sc. (IT) Examination

1st Semester

INTRODUCTION TO DIGITAL LOGIC

Full Marks- 70   Pass Marks- 21   Time- 3 hours

The figures in the margin indicate full marks.

PART – A

Q.1. Answer all questions: **(16x1=16)**

a) Convert $(1100101011.1110)_2$ to hexadecimal equivalent.

b) Convert $(3000.45)_{10}$ into its equivalent octal number.

c) Which gates are called as Universal Gates?

d) Find the dual of following Boolean expression: (A+B)(A+C)=A+BC

e) What is a full adder?

f) What is a parity bit generator?

g) What is a demultiplexer?

h) What is a decoder?

i) Draw the logic diagram for a gated S-R Latch

j) What is a flip-flop?

k) What are the two basic types of counters?

l) Give some applications of shift registers.

m) Name the three types of TTL gates.

n) Which is the fastest and the slowest logic family?

o) Give the classification of logic families.

p) What is propagation delay?

PART – B

Q.2. Answer all questions: **(4x3.5=14)**

     a) What is Duality theorem? Reduce the expression: $f=A[B+\overline{C}\ (\overline{(AB + A\overline{C})}]$

     b) Give the comparison between combinational and sequential circuits.

     c) Using K-map, simplify the following function: $F(a,b,c,d)=\sum(1,4,6,7,8,9,10,11,15)$

     d) Explain the function of 3-input TTL NAND gate.

PART – C

Q.3. State and prove De-Morgan's Theorem.   **(10)**

OR

Minimize the following logic function using Quine-Mc-Cluskey method: $(A,B,C,D)=\sum m(0,1,2,3,5.7.8.9,11,14)$ **(10)**

Q.4. Explain the look ahead carry generators and discuss its utility in adders.   **(10)**

OR

Implement a full adder circuit using two half adders.   **(10)**

Q.5. Explain the working of a master-slave JK flip flop. Explain how it overcomes race-around condition.   **(10)**

OR

Explain the operation of Serial-in-Serial-out shift register.   **(10)**

Q.6. Explain the working of NAND gate using n-channel MOS logic circuit.   **(10)**

OR

With the help of logic diagram and circuit diagram explain static RAM cell.   **(10)**