**SUBJECT CODE = CSE024105**

Roll No. of candidate

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**2017**

**End Semester M.Tech Examination**

**1st Semester**

**FUNDAMENTALS OF COMPUTER SYSTEMS**

Full Marks- 70          Pass Marks- 21          Time- 3 hours

*The figures in the margin indicate full marks.*

**PART A**

**Q 1. Answer all questions:** (16x1=16)

a) Where does the assembler store the object code?

b) In which addressing mode operand value is directly specified?

c) What is pipelining?

d) What are the three types of CPU organization basically most computers fall into?

e) Does the kernel remain aware of user threads?

f) Consider a set of n tasks with known runtimes $r_1, r_2, \ldots, r_n$ to be run on a uniprocessor machine? Which of the scheduling algorithms will result in maximum throughput?

g) Where is the control transferred after the interrupt breaks the execution of instructions?

h) How can a deadlock arise?

i) Draw the waveform for: $X = A \sin(2\pi ft + \emptyset)$ where A=0.5, f = 2 and $\emptyset$ =0

j) Give the vital difference between packet switching and circuit switching.

k) How are the frames in a LAN transmitted to another LAN?

l) What is IP addressing?

m) Give the difference between synthesized and inherited attributes.

n) Consider the following C program and find the tokens:

```
int min( i, j )
{
    int i,j;
    return i > j ? i : j;
}
```

o) Associate semantic rules for the following grammar:

$E \rightarrow E + T / T$

$T \rightarrow T*F / F$

$F \rightarrow (E) / id$

p) Construct the DAG for :

**a + a \* ( b – c ) + ( b – c ) \*d**

## PART B

**Q 2.** **(4x3.5=14)**

a) A computer system supports one address and two address instructions and the word size is **16 bits**. Main memory is **64 words**. If there are **8 two address instructions** then how many one address instructions are used?

b) Explain time slicing. How its duration affects the overall working of the system?

c) Consider a network of bandwidth **1 MHz** and SNR of **24 db**. Calculate the capacity of the channel. Also find how many signalling levels are required.

d) Consider the following code fragment. Generate the three-address code for it.

**for ( j = 1; j <= 10; j++)**

**if x = y then a=b+c**

## PART C

**Q 3.** Explain the instruction format in detail. **(10)**

### OR

Give the differences between micro program control unit and hard wired control unit. **(10)**

**Q 4.** Assume you have the following jobs to execute with one processor, with the jobs arriving in the order:

| i: | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| Burst time: | 70 | 10 | 20 | 12 | 60 |

Use FCFS and Round Robin scheduling (quantum = 30) and calculate the average waiting time for the processes. Also calculate the turnaround time for process P3 in each case. **(10)**

**OR**

Apply FIFO and LRU page replacement algorithms. Use 3 frames and consider the following reference string. Find the number of page faults. **(10)**

**5, 2, 4, 6, 1, 3, 6, 4, 1, 3, 5, 1.**

**Q 5.** Explain TCP/IP model. Compare it with OSI model. **(10)**

**OR**

Define modulation. Explain its different types in detail. **(10)**

**Q 6.** Construct the predictive parsing table for the given grammar using first( ) and follow( ). Also find if it is LL(1) parsing. **(10)**

*E →TA*

*A → + TA / ε*

*T → FB*

*B → *FB / ε*

*F → ( E ) / id*

**OR**

Describe the phases of the compiler design with a figure. **(10)**